UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/770,470	02/04/2004	Shigehiko Saida	03180.0352	1365

22852 7590 08/23/2005

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/770,470	SAIDA ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 17* is/are pending in the application.

4a) Of the above claim(s) *9 - 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/04/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of **Group I**, claims **1 – 8** in the reply filed on July 06, 2005 is acknowledged.

2. Claims **9 – 17** withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected **Group II**, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on July 06, 2005.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on February 04, 2004.

Information Disclosure Statement

4. This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on February 04, 2004.

The references cited on the PTO -1449 form have been considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims **1 – 5** and **7** are rejected under 35 U.S.C. 102(e) as being anticipated by Wurster (US Patent No. 6,928,191).

7. Regarding claim **1**, Wurster discloses a DRAM device comprising:

a semiconductor substrate 101 (fig. 6) having a first conductivity type (p-type; column 3, lines 40 – 44) and including an side wall and a bottom face (generally indicated as bottom of the trench) enclosed by the side wall;

a plate electrode 165 (fig. 6, column 3, lines 60 – 61) having a second conductivity type different from the first conductivity type (n-type; column 7, lines 65 – 67), wherein the plate electrode is provided from the bottom face to the side wall in the semiconductor substrate 101;

a capacitor insulating film 164 (fig. 6; column 4, lines 1 – 2) provided on the bottom face and the side wall;

a collar oxide film 168 (fig. 6; column 4, lines 33 – 34)) provided on the side wall, a ring-shaped lower end of the collar oxide film being in contact with the capacitor insulating film 164 and the collar oxide film 168 is in contact with the plate electrode 165 (fig. 6);

a storage electrode 161 (fig. 6; column 2, lines 27 – 30 and column 3, lines 61 – 67.) provided on the plate electrode 165 and the capacitor insulating film 164, a height of an upper surface of the storage electrode 161 is higher than a height of an upper end of the collar oxide film 168;

a buried strap or capacitor extraction electrode 162 (fig. 6; column 4, lines 56 – 60. *Note that the buried strap 162 has a same function as the capacitor extraction electrode designated*

in the claimed invention. For examination purpose "162" is referred to as a capacitor extraction electrode) provided on the upper end of the collar oxide film 168 and on the upper surface of the storage electrode 161, the capacitor extraction electrode 162 being electrically connected to the storage electrode 161 and in contact with an upper part of the side wall 201 (fig. 6, column 4, lines 56 – 58); and

a buried contact or buried strap region 250 (fig. 6, line 65). *Note that the buried contact 250 has a same function as buried strap region designated in the claimed invention. For examination purpose "250" is referred to as a buried strap region;* provided within the semiconductor substrate 101 including the upper part of the side wall, the buried strap region 250 being in contact with the collar oxide film (at the corner of 201 and collar oxide film 168 (fig. 6)) and electrically connected to the capacitor extraction electrode 162, the buried strap region 250 having the second conductivity type (n-type; column 17, lines 29 – 31).

Regarding claim **2**, Wurster discloses the claimed invention of claim 1 and since the collar oxide film 168 is deposited by the same process as disclosed in the instant application (i.e. LPCVD; column 6, lines 50 – 60), the collar oxide film with respect to the side wall would inherently posses identical property as the instant claim which is a tensile stress.

Regarding claims **3** and **4**, Wurster discloses the collar oxide film 168 is deposited by LPCVD (column 6, lines 50 – 60).

Regarding claim **5**, Wurster discloses a height of an interface between the storage electrode 161 (fig. 6) and the capacitor extraction electrode 162 (fig. 6) is higher than that of a plane on which a lower end of the collar oxide film 168 is an outer edge.

Regarding claim **7**, Wurster discloses the storage electrode 161 (figs. 8 and 12) having a width at a side wall in contact with the capacitor insulating film is larger than that at a side wall in contact with the collar oxide film (column 14, lines 11 – 13 and column 15, lines 4 – 6).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim **6** rejected under 35 U.S.C. 103(a) as being unpatentable over Wurster (US Patent No. 6,928,191) in view of Schrems et al. (US Patent No. 6,376,348).

10. Regarding claim **6**, Wurster discloses the claimed invention of claim 1 and further the device comprising:

an isolation region 180 (fig. 6; column 4, lines 44 – 45) provided on the capacitor extraction electrode 162;

a drain region 113 (fig. 6; column 4, line 62) provided within the semiconductor substrate 101 including an upper surface of the semiconductor substrate 101, wherein the drain region having the second conductivity type (n-type; column 4, lines 62 – 64);

a gate insulating film (not shown; column 10, lines 7 – 10) provided on the upper surface of the semiconductor substrate 101;

a gate electrode 112 (fig. 6; column 4, lines 61 – 67 and column 10, lines 7 – 10) provided on the gate insulating film and above the drain region 113 (fig. 6; column 4, lines 61 - 67);

a source region 114 (fig. 6); column 4, lines 61 – 67 and column 10, line 22) provided under the gate insulating film, below the gate electrode, and separate from the drain region 113 within the semiconductor substrate 101 including the upper surface of the semiconductor substrate 101, wherein the source region is electrically connected to the buried strap region 250 and having the second conductivity type (n-type; column 4, lines 62 – 64) ; and

a bit line 185 (fig. 6; column 5, line 13) electrically connected to the drain region 113.

Note that Wurster designates diffusion region 113 as a drain region connected to bit line 185 and diffusion region 114 as a source region connected to buried strap region 250, the instant claim 6 calls for the opposite in designating regions 113 and 114.

Wurster does not explicitly show the drain region 113 is electrically connected to the buried strap region 250; and the bit line electrically 185 connected to the source region 114 as the claimed invention of the instant claim. .

However, it is commonly known in the semiconductor technology that the terms source and drain are interchangeable depending on the direction of the current flow as shown by Schrems (column 2, lines 54 – 60. *Note that Schrems is one of the inventors of the cited prior art reference No. 6,928,191).* Thus, regions 113 and 114 read on the claimed source and drain respectively.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to designate the source 114 and drain 113 of Wurster with the interchangeable designated source as 113 and designated drain as 114 depending on the direction of the current flow as shown by Schrems in order to have a device with the drain region being electrically connected to the buried strap region and the bit line connected to the source region as the claimed invention of the instant claim.

11. Claims **8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wurster (US Patent No. 6,928,191) in view of Chudzik et al. (US Patent No. 6,770,526).

12. Regarding claim **8**, Wurster discloses the claimed invention of claim 1 but fails to teach irregularities provided on the bottom face and on the side wall of the semiconductor substrate.

However, Chudzik shows trench 102 (figs. 6 – 8) having irregularities provided on the bottom face and on the side wall of the semiconductor substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the trench capacitor of Wurster with irregularities provided on the bottom face and on the side wall of the semiconductor substrate as shown by Chudzik in order to increase the capacitance of the capacitor (column 2, lines 58 – 63).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kudelka et al. (US Patent Application Publication No. 2003/0194867) and Tsunashima et al. (US Patent No. 6,326,658) disclose a

semiconductor device similar to that of Wurster (US Patent No. 6,928,191), Schrems et al. (US Patent No. 6,376,348) and Chudzik et al. (US Patent No. 6,770,526).

14. A shortened statutory period for response to this action is set to expire e (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

August 15, 2005